a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

an electrically conductive unbiased layer provided on a back side of said substrate for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

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66. (Amended) A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

an electrically conductive unbiased layer provided on a back side of said substrate for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

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92. (Cancel without disclaimer or prejudice)

94. (Cancel without disclaimer or prejudice)

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96. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate; and

an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer forming an electrical path for removing unwanted voltages and

electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

97. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and said bias voltage source thereby removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

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98. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate;

an electrically conductive unbiased metallic layer provided on a backside of said substrate, said conductive metallic layer wire bonded to a bonding pad of said semiconductor device for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate; and

said bonding pad forming an electrical path between said conductive metallic layer and at least one other area of said device.

99. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer in electrical communication with a bonding pad of said semiconductor device for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

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101. (Amended) A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

an electrically conductive unbiased layer provided on a back side of said substrate for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

102. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and said bias voltage source for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

103. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer;

an electrically conductive unbiased metallic layer provided on a backside of said substrate, said conductive metallic layer wire bonded to a bonding pad of said semiconductor device; and

said bonding pad forming an electrical path between said conductive metallic layer and at least one other area of said device for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

104. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer in electrical communication with a bonding pad of said semiconductor device for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.